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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/039,765
Filing Date: November 07, 2001
Appellant(s): ROCHE ET AL.

Michael W. Taylor
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 5, 2008 appealing from the Office action mailed November 1, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

SPI Block Guide, V 3.06, Freescale Semiconductor, Inc., January 21, 2000

System Management Bus Specification, Version 2.0, SBS Implementers Forum, August 3, 2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 20-43 and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over SPI Block Guide(hereinafter referred to as SPI), in view of System Management Bus (SMBus) Specification(hereinafter referred to as SMB).

Regarding claim 20, SPI discloses a method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value(SCK=1), the method comprising: providing one of the devices with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value(Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the one of the devices, after data is applied to the data line(Figure 4-2, Data is applied before SCK Edge Nr. 1); and maintaining the data on the data line by the device sending the data(Figure 4-2, Data is applied until rising edge of clock).

SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent and releasing the clock. However, SMB discloses maintaining the tie to the clock line by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters. The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions in SPI and the clock only transitions when the slave release the clock in SMB.

Regarding claim 21, SPI discloses a method wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted(Figure 4-2).

Regarding claim 22, SPI discloses a method wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device(Figure 4-2, Data is applied before SCK Edge Nr. 1).

Regarding claim 23, SMB discloses a method wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(Section 4.3.3, Figure 4-7).

Regarding claim 24, SMB discloses a method wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Page 22, Section 4.3.3, Figure 4-7).

Regarding claim 25,Regarding claim 25, SPI discloses a method wherein the master device ties the clock line to the second logic value when the master receives data from the slave device(Figure 4-2).

Regarding claim 26, SMB discloses a method wherein the slave device detects the second logic value on the clock line then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device(Section 4.3.3, Figure 4-7).

Regarding claim 27, SMB discloses a method wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line(Section 4.3.3, Figure 4-7).

Regarding claim 28, SPI discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 4-2).

Regarding claim 29, SMB discloses a method further comprising providing the slave device with a communication interface circuit including: a trigger for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value; an input for applying a clock line release signal to the trigger; and an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger and a second value when the clock line is released by the trigger(Section 4.3.3, Figure 4-7).

Regarding claim 30, SPI discloses a method, wherein the communication interface circuit further comprises: storage for storing at least one data; and means for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value(Figure 4-3).

Regarding claim 31, SPI discloses a method, wherein the first logic value is 1 and the second logic value is 0(Figure 4-2).

Regarding claim 32, SPI discloses a method of transmitting data between two devices connected via a clock line and at least one data line, the method comprising: maintaining the clock line on a first logic value by default(SCK=1); providing one of the devices with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value(Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the one of the devices, after data is applied to the data line(Figure 4-2, Data is applied before SCK Edge Nr. 1); and maintaining the data on the data line by the device sending the data(Figure 4-2, Data is applied until rising edge of clock).

SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent and releasing the clock. However, SMB discloses maintaining the tie to the clock line by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters. The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions and the clock only transitions when the slave release the clock.

Regarding claim 33, SPI discloses a method, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted(Figure 4-2).

Regarding claim 34, SPI discloses a method, wherein the master device ties the clock line to the second logic value after applying data the data line when the master device is sending the data to the slave device(Figure 4-2, Data is applied before SCK Edge Nr. 1).

Regarding claim 35, SMB discloses a method, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(Section 4.3.3, Figure 4-7).

Regarding claim 36, SMB discloses a method, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Section 4.3.3, Figure 4-7).

Regarding claim 37, SPI discloses a method, wherein the master device ties the clock line to the second logic value when the master receives data from the slave device(Figure 4-2).

Regarding claim 38, SMB discloses a method, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device(Section 4.3.3, Figure 4-7).

Regarding claim 39, SMB discloses a method wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line(Section 4.3.3, Figure 4-7).

Regarding claim 40, SPI discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 4-2).

Regarding claim 41, SMB discloses a method providing the slave device with further a communication comprising interface circuit including: a trigger circuit for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value; an input for applying a clock line release signal the trigger circuit; and an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger circuit and a second value when the clock line is released by the trigger circuit(Section 4.3.3, Figure 4-7).

Regarding claim 42, SPI discloses a method wherein the communication interface circuit further comprises: a buffer for storing at least one data; and a circuit for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value(Figure 4-3).

Regarding claim 43, SPI discloses a method wherein the first logic value is 1 and the second logic value is 0(Figure 4-2).

Regarding claim 48, SPI discloses a synchronous data transmission system comprising: a clock line; a data line; a master data transmitting/receiving comprising a clock line connection terminal for connection to a clock line; at least one data line connection terminal for connection to a data line(page 27, Figure 4-2); a circuit for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high)(Page 27, Figure 4-2, SCK changes from 1 to 0 at SCK Edge Nr. 1); and data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value(Figure 4-2, Data is applied before SCK Edge Nr. 1), then releasing the clock line, and maintaining the data, when the data is to be sent(Figure 4-2) and a slave data transmitting/receiving comprising a clock line connection terminal connected to the clock line; at least one data line connection terminal connected to the data line and means for detecting a change from the first logic value to the second logic value on the clock line, and reading the data on the data line, when the data is to be received(Figure 4-2).

SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent and releasing the clock. However, SMB discloses maintaining the tie to the clock line by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters. The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions and the clock only transitions when the slave release the clock.

Regarding claim 49, SPI discloses a system, wherein the master device further comprises data receiving unit for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading data on the data line, then releasing the clock line, when the data is to be received by the master device(Figure 4-2).

Regarding claim 50, SMB discloses a system, wherein the slave device further comprises means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line the second logic value, applying the data to the data line, and releasing the clock line, when the data is to be sent from the slave device(Page 22, Section 4.3.3, Figure 4-7).

Claims 44-46 are rejected under 35 U.S.C. 102(a) as being anticipated by SPI.

Regarding claim 44, SPI discloses a data transmitting/receiving device comprising: a clock line connection terminal for connection to a clock line; at least one data line connection terminal for connection to a data line(page 27, Figure 4-2); a circuit for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high)(Page 27, Figure 4-2, SCK changes from 1 to 0 at SCK Edge Nr. 1); and a data sending unit for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value(Figure 4-2, Data is applied before SCK Edge Nr. 1), then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent(Figure 4-2).

Regarding claim 45, SPI discloses a device, further comprising a data receiving unit for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading data on the data line, then releasing the clock line, when the data is to be received(Figure 4-2).

Regarding claim 46, SPI discloses a data transmitting/receiving device comprising: a clock line connection terminal for connection to a clock line, the clock line being maintained by default on a first logic value(SCK=1); at least one data line connection terminal for connection to a data line(page 27, Figure 4-2); a circuit for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value(Page 27, Figure 4-2, SCK changes from 1 to 0 at SCK Edge Nr. 1); a detector for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, and reading data on the data line, and releasing the clock line, if data is to be received(Figure 4-2), or applying data to the data line, and releasing the clock line if the data is to be sent(Figure 4-2, Data is applied before SCK Edge Nr. 1).

Claims 51 and 52 are rejected under 35 U.S.C. 102(a) as being anticipated by SMB.

Regarding claim 51, SMB discloses a communication interface circuit for connection to a data transmitting/receiving device via a clock line and at least one data line, the circuit comprising: a circuit for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value; a trigger for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value(Page 22, Section 4.3.3, The clock is stretched low periodically); an input to apply a clock line release signal to the trigger(The clock is released when slave is done); and an output to deliver an information signal that has a first value(low=0) when the clock line is tied to the second logic signal by the trigger and a second value(high=1) when the clock line is released by the trigger(Page 22, Section 4.3.3, Figure 4-8).

Regarding claim 52, SMB discloses a communication interface circuit further comprising: storage for storing data; and an applicator for automatically applying the data to the data line

when the clock line changes from the first logic value to the second logic value(Section 4.3.3, Figure 4-7).

(10) Response to Argument

Arguments regarding independent claims 20, 32 and 48:

In response to Appellant's arguments against the references individually, Examiner notes that the combination of SPI and SMB disclose the claimed invention. SPI discloses a method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value(SCK=1), the method comprising: providing one of the devices with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value(Page 27, Figure 4-2, SCK=0 at SCK Edge Nr. 1); tying the clock line to the second logic value, via the one of the devices, after data is applied to the data line(Figure 4-2, Data is applied before SCK Edge Nr. 1); and maintaining the data on the data line by the device sending the data(Figure 4-2, Data is applied until rising edge of clock). SPI does not specifically disclose maintaining the tie to the clock line by the device to which the data is sent and releasing the clock. However, SMB discloses maintaining the tie to the clock line by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7). It would have been obvious to one of ordinary skill in the art to have the device receiving data to hold the clock down, as disclosed by SMB, in the method of SPI, since this would allow clock synchronization to allow slower slave devices to cope with faster masters. The combination of SPI and SMB would implicitly maintain data on the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions in SPI and the clock only transitions when the slave release the clock in SMB.

In response to Appellant's argument that SPI does not disclose the clock line maintained by default on a first logic value, Examiner respectfully disagrees. As noted above, SPI discloses

when CPOL =1, active low clock is selected and the idle, i.e. default, value is SCK=High=1(Page 17, CPOL – SPI Clock Polarity Bit).

In response to Appellant's argument that SPI does not disclose each device provided with the ability to tie the clock line to a potential representing a second logic value opposite of the first logic value, Examiner notes that SPI and SMB together show this feature. SPI discloses a device(master) provided with the ability to tie the clock to a potential representing a second logic value(SCK=Low=0) opposite of the first logic value at SCK Edge Nr. 1(Figure 4-2) and SMB discloses a device(slave) with the ability to tie the clock to a potential representing a second logic value(SMBCLK=0) opposite of a first logic(SMBCLK=0)(Page 22, Section 4.3.3, Figure 4-7).

In response to Appellant's argument that SPI does not disclose the two devices tying the clock line to the second logic value after data is applied, Examiner notes that SPI and SMB together show this feature. SPI discloses the master tying the clock line to the second logic value, via the one of the devices, after data is applied to the data line (Figure 4-2, Data is applied before SCK Edge Nr. 1) and SMB discloses the slave tying the clock line to the second logic value after data is applied to the data line(Page 22, Section 4.3.3, Figure 4-7).

In response to Appellant's argument that SPI does not disclose the tying of the clock line is maintained by the device(slave) to which data is sent while the device has not read the data, Examiner notes that this feature is taught by SMB. SMB discloses maintaining the tie to the clock line by the device to which the data is sent(Page 22, Section 4.3.3, Figure 4-7).

In response to Appellant's argument that SPI does not disclose the data on the data line is maintained by the device(master) sending the data at least until an instant when the clock line is released by the device(slave) to which data is sent, Examiner notes that SPI and SMB together show this feature. The combination of SPI and SMB would implicitly maintain data on

the data line by the sending device until an instant after the slave releases the clock line since the data changes only on clock transitions in SPI(Figure 4-2, data on MOSI pin changes when clock(CPOL =1) transitions from 0 to 1; see al) and the clock only transitions when the slave release the clock in SMB(Figure 4-7).

In response to Appellant's argument that SMB does not disclose slave tying the clock line to the second logic value opposite of the first logic value, Examiner respectfully disagrees. SMB does disclose a slave with the ability to tie the clock to a potential representing a second logic value(SMBCLK=0) opposite of a first logic(SMBCLK=0)(Page 22, Section 4.3.3, Figure 4-7).

In response to Appellant's argument that SMB does not disclose the tie to the clock being maintained by the device(slave) to which data is sent while the device has not read the data because the slave must comply with a timeout, Examiner respectfully disagrees. SMB discloses that the slave must adhere to timeout parameter. This timeout enables the master or slave to conclude that a defective device is holding the clock low indefinitely(Page 13, Section 3.1.1.3). However, during normal operation, i.e. no defective devices, the slave can maintain the tie to the clock to stretch the low period of the clock and therefore meets the claim language. The claim language does not require devices without timeout values. Thus, Appellant's argument is not persuasive.

Arguments regarding independent claims 44 and 46:

In response to Appellant's argument that SPI does not disclose tying the clock line to a potential representing a second logic value that is the opposite of a first logic value and waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value, then releasing the clock line, and maintaining the data on the data line at

least until the clock line has the first logic value, when the data is to be sent, Examiner respectfully disagrees. SPI does disclose Regarding claim 44, SPI discloses tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high)(Page 27, Figure 4-2, CPOL=1, SCK changes from 1(idle state) to 0 at SCK Edge Nr. 1); and waiting for the clock line to have the first logic value(CPOL=1, idle state, SCK=1), applying data to the data line(MOSI pin), tying the clock line to the second logic value(Figure 4-2, Data is applied before SCK Edge Nr. 1), then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent(Figure 4-2, Data changes when the clock transitions 0 to 1).

Arguments regarding independent claim 51:

In response to Appellant's argument that SMB does not disclose the tie to the clock being maintained by the device(slave) to which data is sent while the device has not read the data because the slave must comply with a timeout, Examiner respectfully disagrees. SMB discloses that the slave must adhere to timeout parameter. This timeout enables the master or slave to conclude that a defective device is holding the clock low indefinitely(Page 13, Section 3.1.1.3). However, during normal operation, i.e. no defective devices, the slave can maintain the tie to the clock to stretch the low period of the clock and therefore meets the claim language. The claim language does not require devices without timeout values. Thus, Appellant's argument is not persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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